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**B D1012 Pages:**

**Scheme of Valuation/Answer Key**

**(Scheme of evaluation (marks in brackets) and answers of problems/key)**

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY FOURTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), MAY 2019 Course Code: CS202**

**Course Name: COMPUTER ORGANISATION AND ARCHITECTURE (CS,IT)** Max. Marks: 100 Duration: 3 Hours

**PART A *Answer all questions,each carries 3 marks***

**1)** Explain one, two and three address instruction with an example for each. (3) **[Explanation and Example (0.5 + 0.5) marks each]**

A **three- address** instruction has three addresses, two for the source operands and one for the destination operand. **Eg. Add A, B,C; C ← A+B (in some architecture it can be interpreted as A← B+C)**

A **two- address** instruction has only two addresses, of which one address stands for source1 and the other acts both as the source2 and the destination. **Eg. Add A, B; B ← A+B** (Here B is both source2 and destination)

**(in some architecture it can be interpreted as A← A+B)**

A **one- address** instruction has only one address, of which the implicit address not present is the accumulator. An implicit operand is present which is accumulator (Acc) **Eg. Add A; Acc ← A+Acc**

**2)** List the steps involved in invoking a subroutine through the use of a link register. (3) **[Steps involved during call - 2 marks, Steps involved during a return -1 mark]**

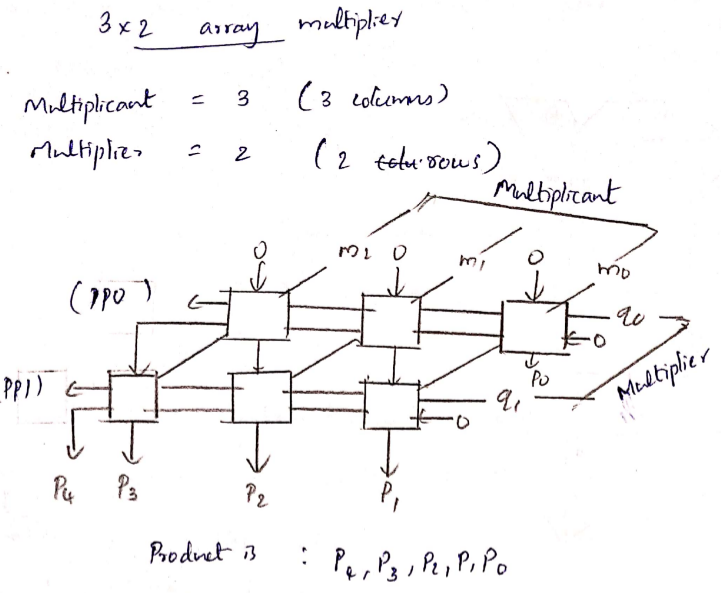
**During call:**

1. LR ← PC (the content of PC is saved to link register)
2. PC← target address

**During return:**

1. PC← LR (the contents of PC must be restored from LR)

**3)** Draw a **3 x 2 array multiplier.**  (3) **[Diagram -3marks]**

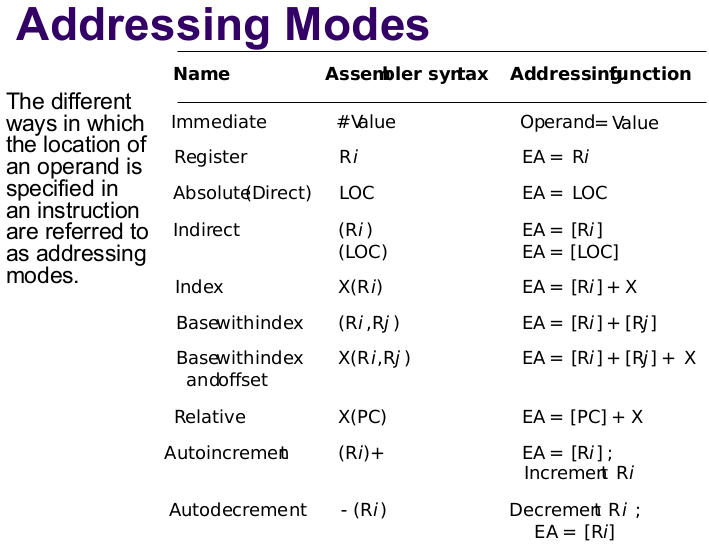


**4)** **Non-restoring division** is faster than restoring division. Justify the statement. (3)

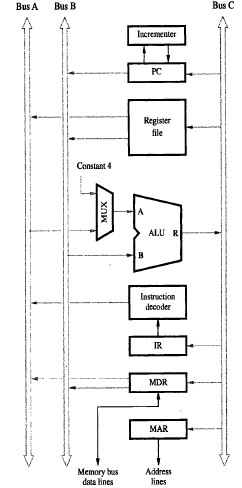
In a restoring division algorithm, the value in register A has to be restored after an unsuccessful subtraction. If A is positive, we shift left and subtract M, i.e., we perform 2A-M. If A is negative, we restore it by performing A+M and then we shift it left and subtract M. This is equivalent to 2A+M. Hence, in a non-restoring division algorithm, the value in A is not restored every time the subtraction is unsuccessful. Hence it is faster than restoring division.

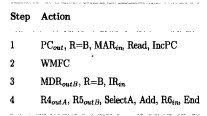
**PART B *Answer any two questions, each carries 9 marks***

**5)** List various addressing modes explain any four with an example for each. (9) **[Listing of at least four addressing modes, Explanation, Example (1 + 4 + 4) marks]**



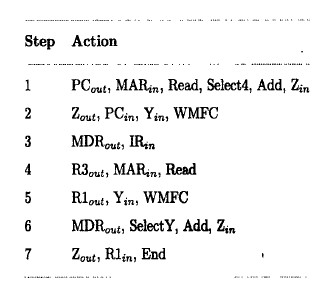
**6 a)** Draw the diagram of a multi-bus organization with 3 buses. Write the control sequence for the instruction Add R4, R5, R6 for the above mentioned multi-bus organization. (5)

 2 marks

 3 marks

**6** **b)** Give the sequence of control steps required to perform the operation Add [R3], R1 in a single-bus organization. (4)

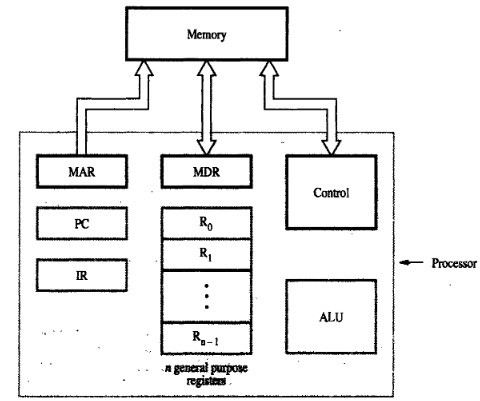
Instruction fetch steps (1 to 3)-----2 marks ; Instruction execution steps( 4 to 7) -----2 marks



**7 a)** Divide (1000)2 by (11)2 using restoring division method. (4)



**7** **b)** Illustrate the basic operational concepts in transferring data between main memory and processor with neat diagram. (5) **[Explanation - 2.5 marks , Figure - 2.5 marks]**

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**Memory read: move contents in memory to processor register**

1. Move the address of the memory location to MAR register
2. Issue read command
3. The contents of memory location is copied to MDR register

**Memory write: move contents in processor register to memory**

1. Move address of memory location to MAR register
2. Move the data to be written to memory to the MDR register
3. Issue write command

**PART C**

***Answer all questions, each carries 3 marks***

**8)** What are vectored interrupts? (3)

* Device identifies itself, sends a special code to processor over bus, typically 4 to 8 bits
* Code supplied by the device may represent a part of the starting address of the interrupt-service routine.

**9)** Give the functions of initiator and target controllers in SCSI bus. (3) **[Initiator controller - 1.5 marks, Target controller - 1.5 marks]**

Initiator controller: it has the ability to select a particular target and send command specifying the operations to be performed. i.e. establish a logical connection with the target controllerTarget controller: (SCSI controller) .

Target controller: The data transfer on the SCSI bus is controlled by the target controller

**10)** Compare synchronous and asynchronous DRAM. (3) **[Comparison bringing out at-least 3 differences]**

1. Synchronous DRAM uses a system clock to coordinate memory accessing while Asynchronous DRAM does not use a system clock to synchronize or coordinate memory accessing.
2. Synchronous DRAM is faster and efficient then asynchronous DRAM.
3. synchronous DRAM provides high performance and better control than the asynchronous DRAM.
4. Modern high-speed PCs uses synchronous DRAM while older low-speed PCs used asynchronous DRAM.
5. Any other relevant points, marks may be awarded

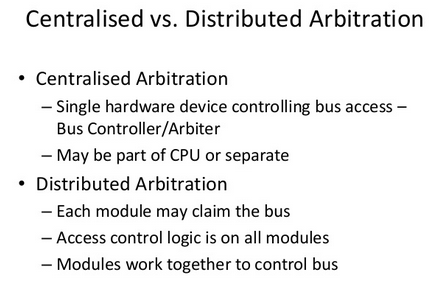
**11)** Define temporal locality and spatial locality. (3) **[Definition (1.5 marks each)]**

· Temporal: a recently executed instruction is likely to be executed again very soon.

· Spatial: Instructions in close proximity to a recently executed instruction (with respect to the instructions’ addresses) are also likely to be executed soon.

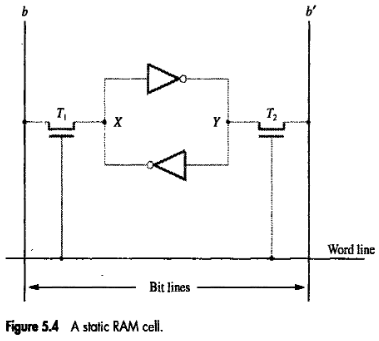
**PART D *Answer any two questions, each carries 9 marks***

**12 a)** Differentiate centralized and distributed bus arbitration mechanism used in DMA. (4) **[Differences - 4 marks]**



Any other relevant points, marks may be awarded

**12b)** Give structure of a typical static RAM cell and explain its read and write operations. (5) **[Structure – 2 marks, operations ( 1.5 marks each)]**



**Read Operation:**

* In order to read the state of the SRAM cell, the word line is activated to close switches T1 and T2.
* The value stored in the latch is available on bit line b and its complement on b’
* Sense / write circuit connected to the bit lines monitors the states of b and b’

**Write Operation:**

* The state of the cell is set by placing the appropriate value on bit line b and its complement on bꞌ
* The word line is then activated so that data is written to the latch
* The required signal on the bit lines are generated by Sense / Write circuit

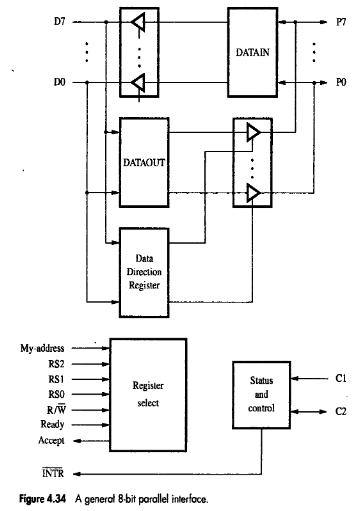
**13)** Differentiate serial port and parallel port. Draw the diagram of a bidirectional 8-bit parallel interface and explain its working. (9) **[Differences - 2 marks, Diagram with explanation (3 + 4)]**

**Parallel port**

* Parallel port transfers data in the form of a number of bits, normally 8 or 16 to or from the device.
* The connection between the device and the computer uses a multiple-pin connector and a cable with as many wires, typically arranged in a flat configuration.
* This arrangement is suitable for devices that are physically close to the computer.

**Serial port**

* Serial port transfers and receives data one bit at a time.
* Suitable for devices at longer distances
* The serial format is much more convenient and cost-effective where longer cables are needed.

Any other relevant points, marks may be awarded

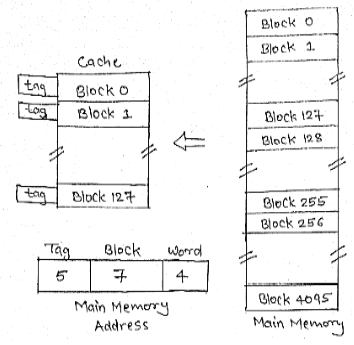
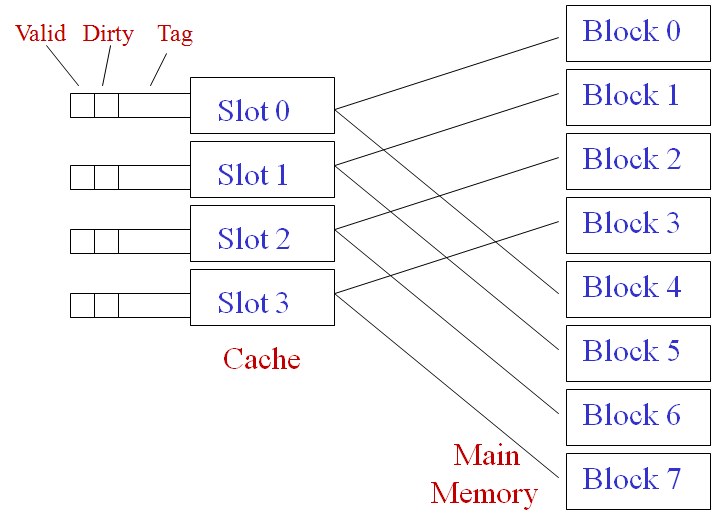
**14)** Elaborate the various cache mapping techniques with an example for each. (9)

**[Direct, Associative, Set Associative – 3 marks each]**

The different Cache mapping technique are as follows:- **a) Direct Mapping b) Associative Mapping c) Set Associative Mapping**

Consider a cache consisting of 128 blocks of 16 words each, for a total of 2048(2K) works and assume that the main memory is addressable by 16 bit address. Main memory is 64K which will be viewed as 4K blocks of 16 works each.

**(a) Direct Mapping:-**

** or simple direct mapping example **

1) The simplest way to determine cache locations in which store Memory blocks is direct Mapping technique.

2) In this block J of the main memory maps on to block J modulo 128 of the cache. Thus main memory blocks 0,128,256,….is loaded into cache is stored at block 0. Block 1,129,257,….are stored at block 1 and so on.

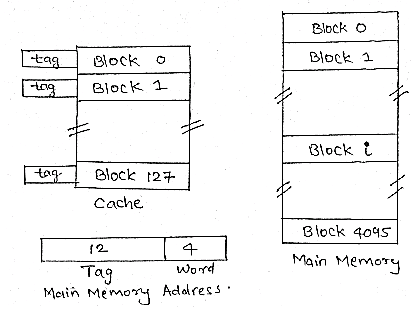
3) Placement of a block in the cache is determined from memory address. Memory address is divided into 3 fields, the lower 4-bits selects one of the 16 words in a block.

4) When new block enters the cache, the 7-bit cache block field determines the cache positions in which this block must be stored.

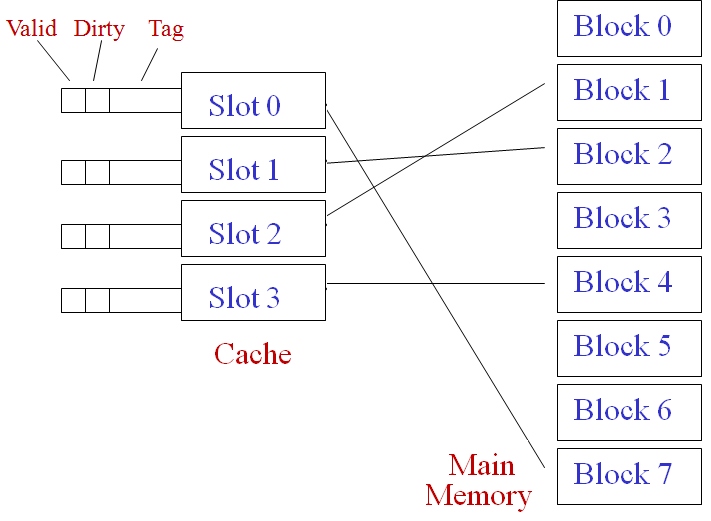
5) The higher order 5-bits of the memory address of the block are stored in 5 tag bits associated with its location in cache. They identify which of the 32 blocks that are mapped into this cache position are currently resident in cache.

6) It is easy to implement, but not Flexible

**(b) Associative Mapping:-**

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**or simple associative mapping**

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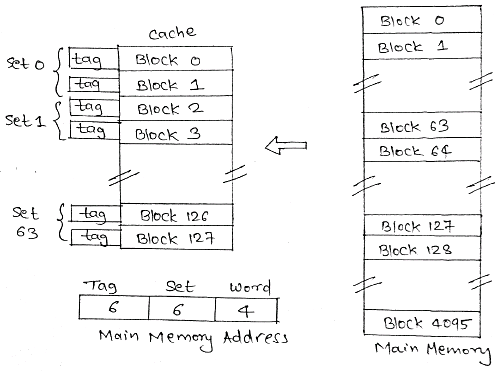
1) This is more flexible mapping method, in which main memory block can be placed into any cache block position.

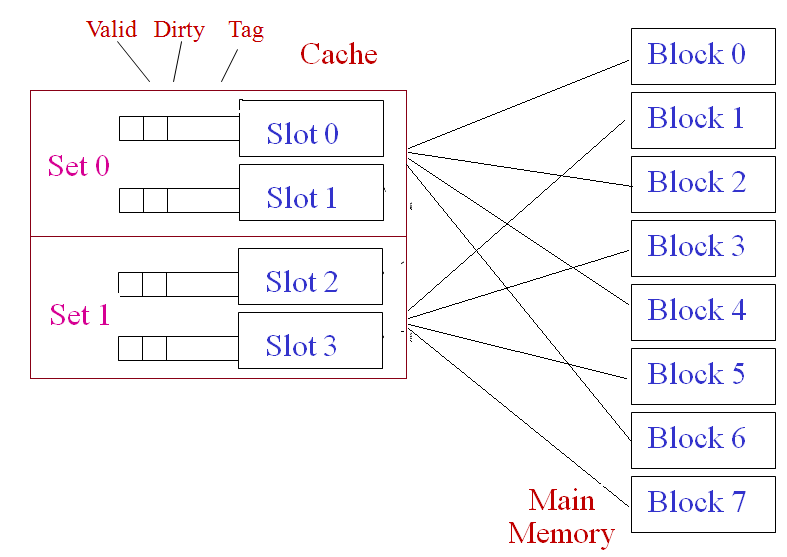
2) In this, 12 tag bits are required to identify a memory block when it is resident in the cache.

3) The tag bits of an address received from the processor are compared to the tag bits of each block of the cache to see if the desired block is present. This is known as Associative Mapping technique.

4) Cost of an associated mapped cache is higher than the cost of direct-mapped because of the need to search all 128 tag patterns to determine whether a block is in cache. This is known as associative search.

**(c) Set-Associative Mapping:-**

** or simple set associative mapping**

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1) It is the combination of direct and associative mapping technique.

2) Cache blocks are grouped into sets and mapping allow block of main memory reside into any block of a specific set. Hence contention problem of direct mapping is eased , at the same time , hardware cost is reduced by decreasing the size of associative search.

3) For a cache with two blocks per set. In this case, memory block 0, 64, 128,…..,4032 map into cache set 0 and they can occupy any two block within this set.

4) Having 64 sets means that the 6 bit set field of the address determines which set of the cache might contain the desired block. The tag bits of address must be associatively compared to the tags of the two blocks of the set to check if desired block is present. This is two-way associative search.

**PART E**

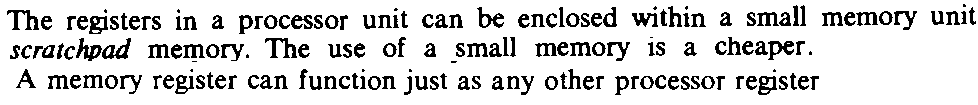
***Answer any four questions, each carries 10 marks***

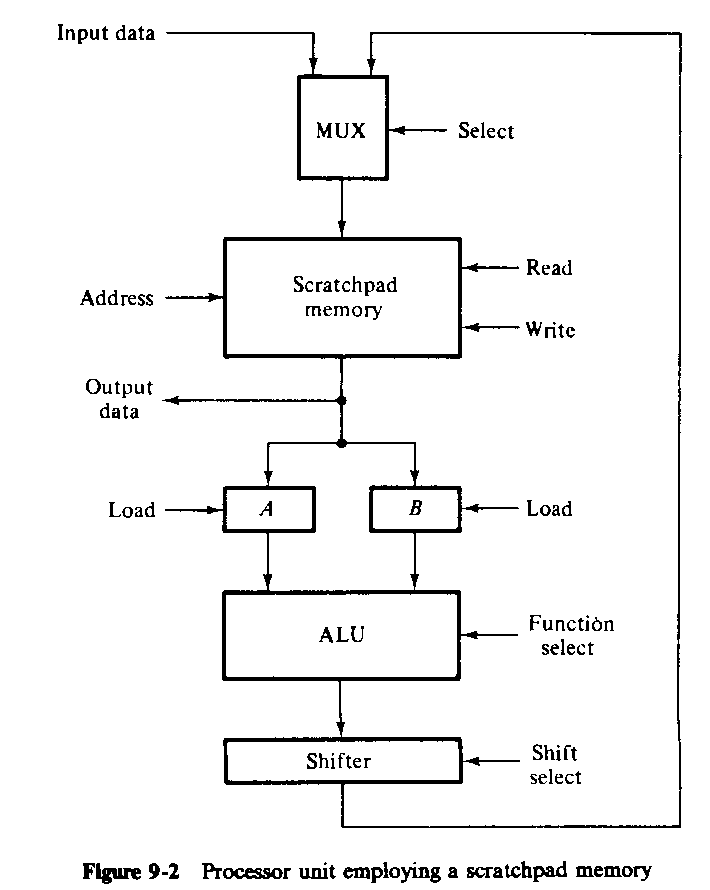
**15 a)** Write the Register Transfer Logic format for a conditional control statement. Give an example and explain the same. (4)

1 mark

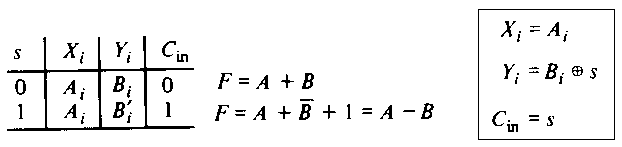
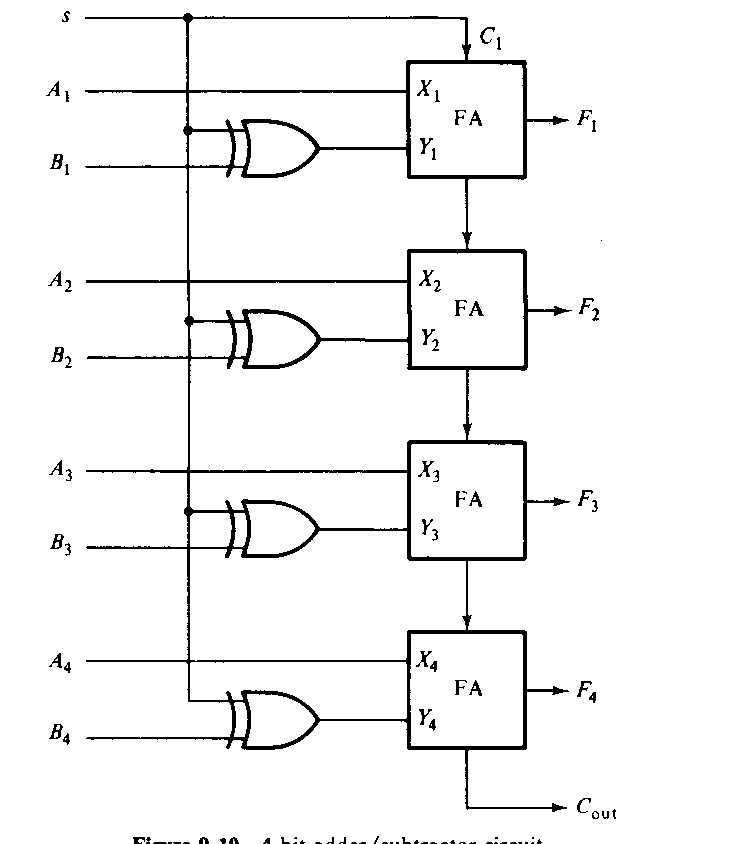
 1.5 marks **[ P - 1 mark + T2 - 1.5 marks + Explanation - 1.5 marks]**

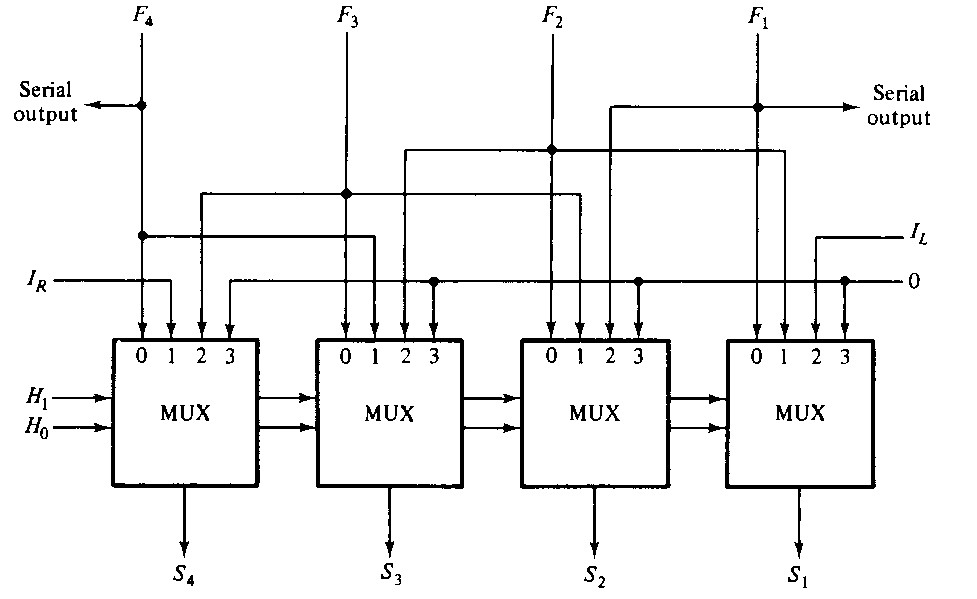
**15 b)** Mention the advantages of using a scratch pad memory. Draw the diagram of a processor that employs a scratch pad memory and explain the same. (6) **[Advantages – 2 marks; Diagram – 2 marks; Explanation – 2 marks]**

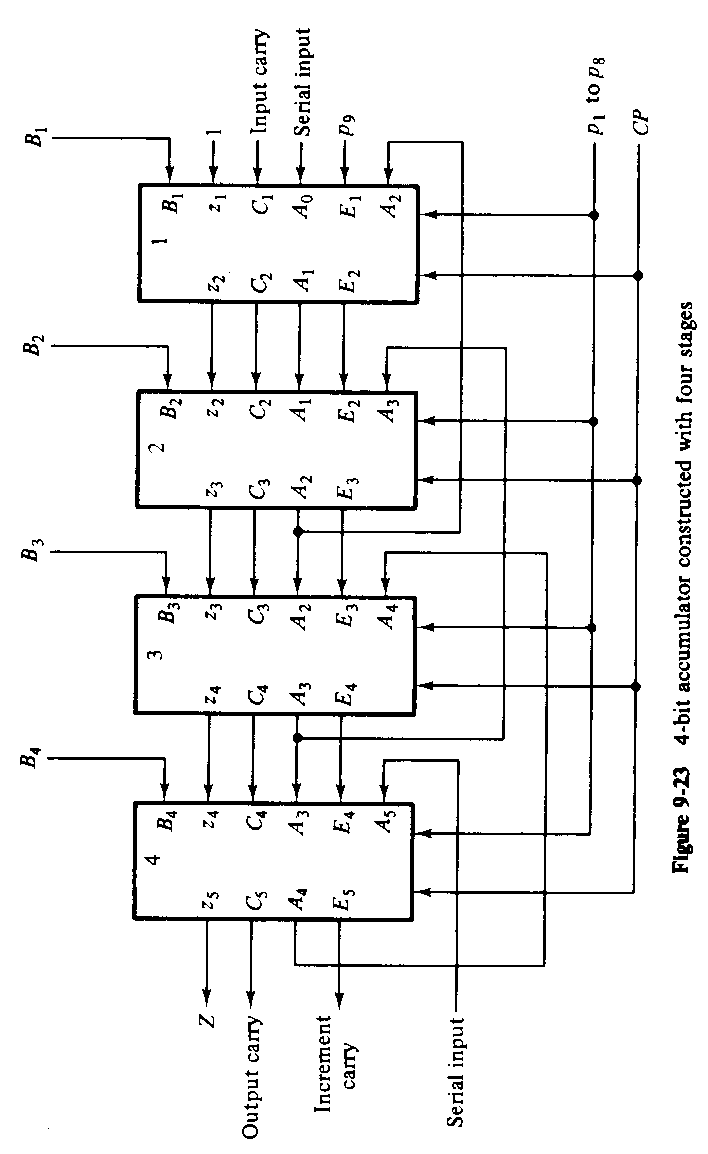




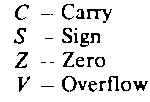
**16 a)** Design an adder/subtractor circuit with one selection variable *s* and two inputs *A* and *B*. When *s* = 0 the circuit performs *A* + *B*. When *s* = 1 the circuit performs *A* – *B* by taking 2’s complement of *B*. (5)

**[ Equations-3 marks + circuit - 2 marks]** 

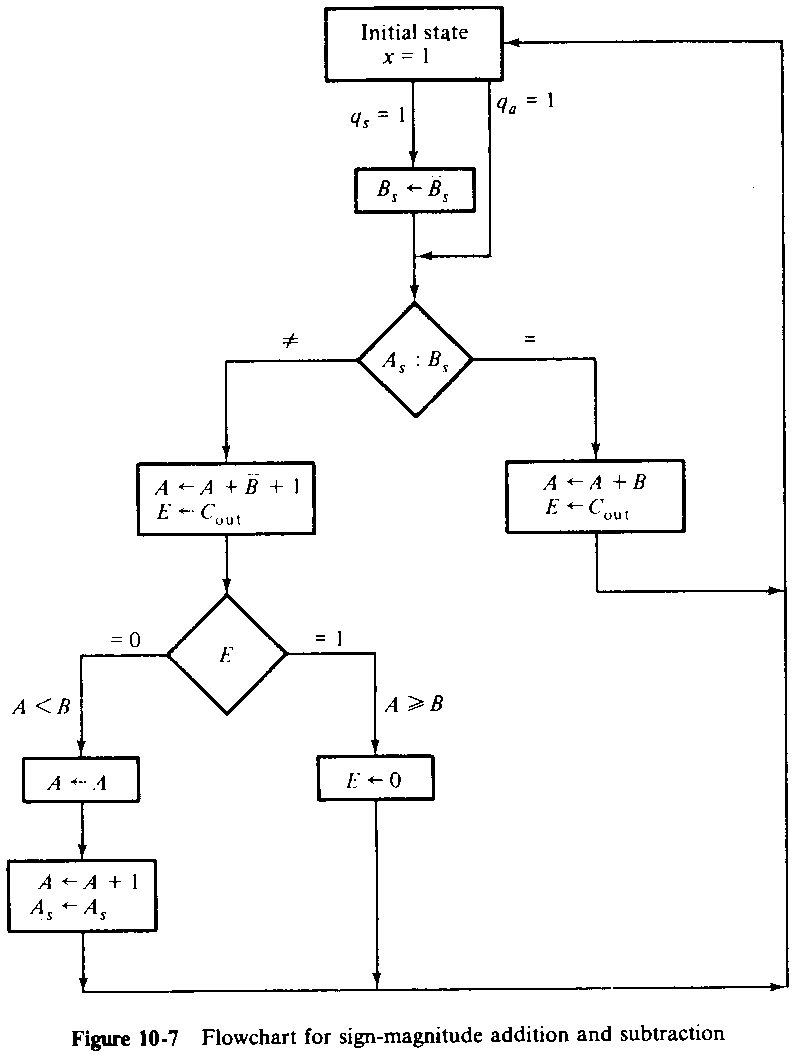
**16 b)** Design a 4-bit combinational logic shifter with 2 control signals H1 and H0 that performs the following operations (bit values given in parentheses are the values of control variables H1 and H0 respectively):- No shift (00), Shift-right (01), Shift- left (10), Transfer 0’s to S (11). (5) **[Diagram – 3 marks; Explanation – 2 marks]** 

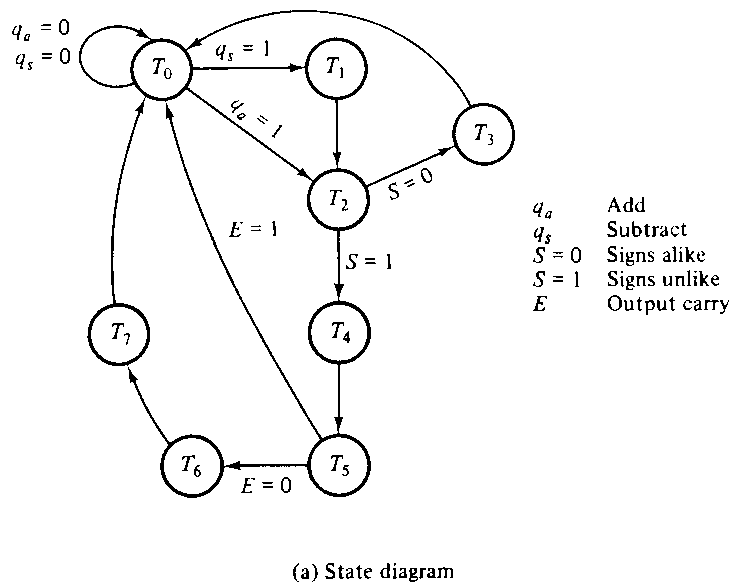
**17 a)** Draw and explain the block diagram for a 4-bit complete accumulator (6) **[Diagram -3 marks, Explanation - 3 marks] **

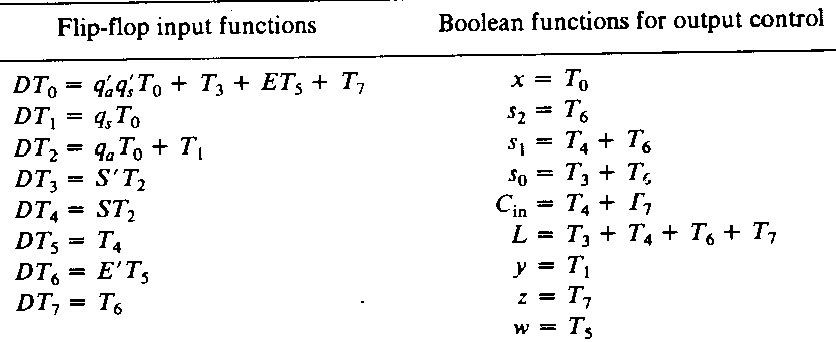
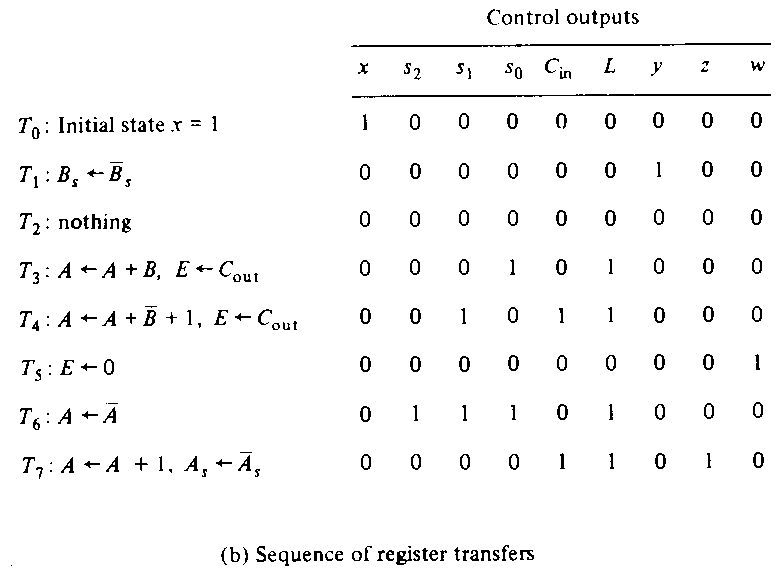
**17 b)** Discuss about condition code bits in a 4 bit status register (4) **[Explanation (1 mark for each bit)]**

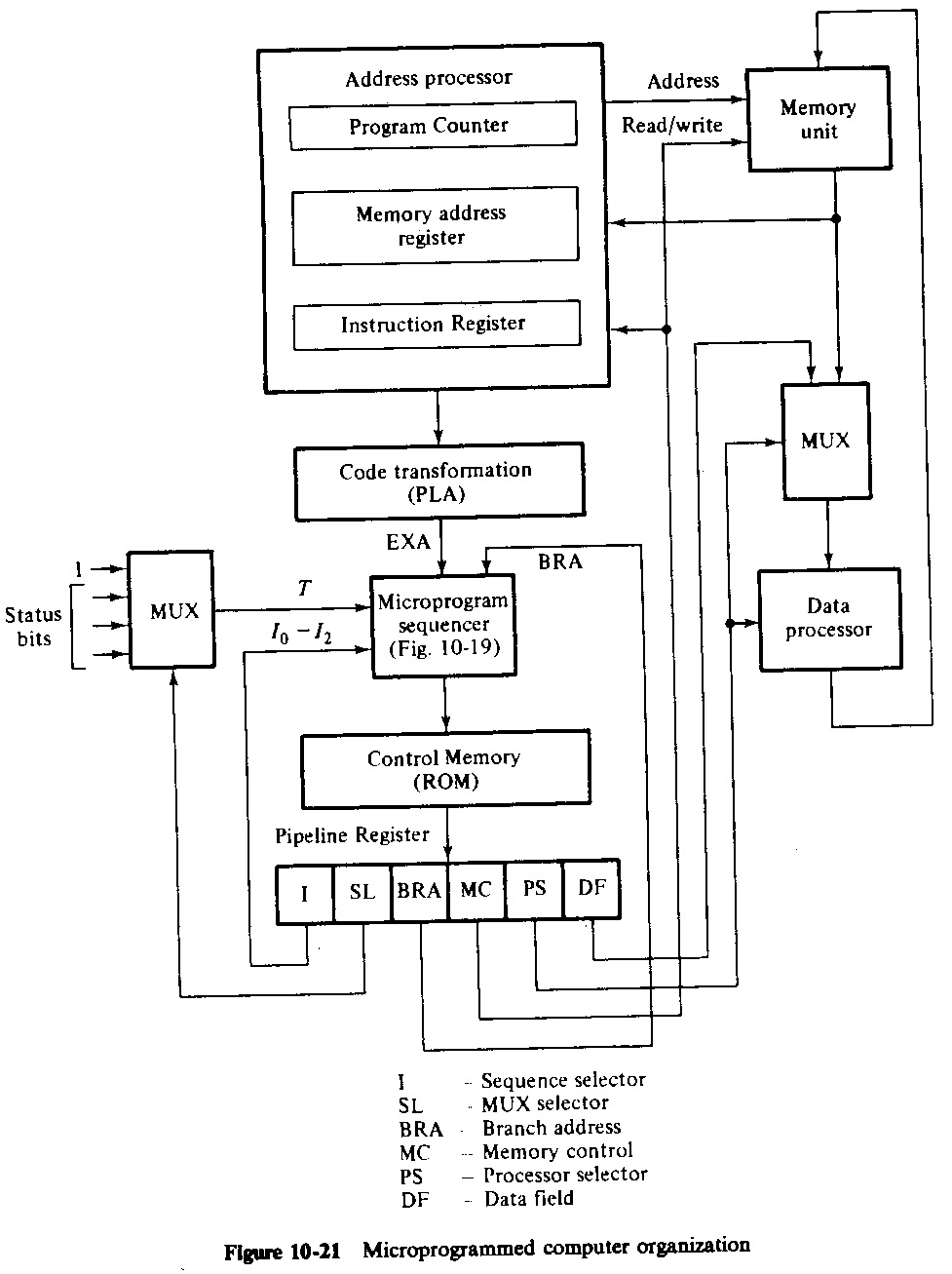
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**18)** Design a hard-wired control unit based on the one flip-flop per state method to add/subtract 2 signed numbers represented in the sign-and-magnitude form. (10) **[Flowchart – 2 marks; State diagram – 2 marks; RTL for each micro-operation – 3 marks; Flip-flop input functions and Boolean functions for control output – 3 marks ]**

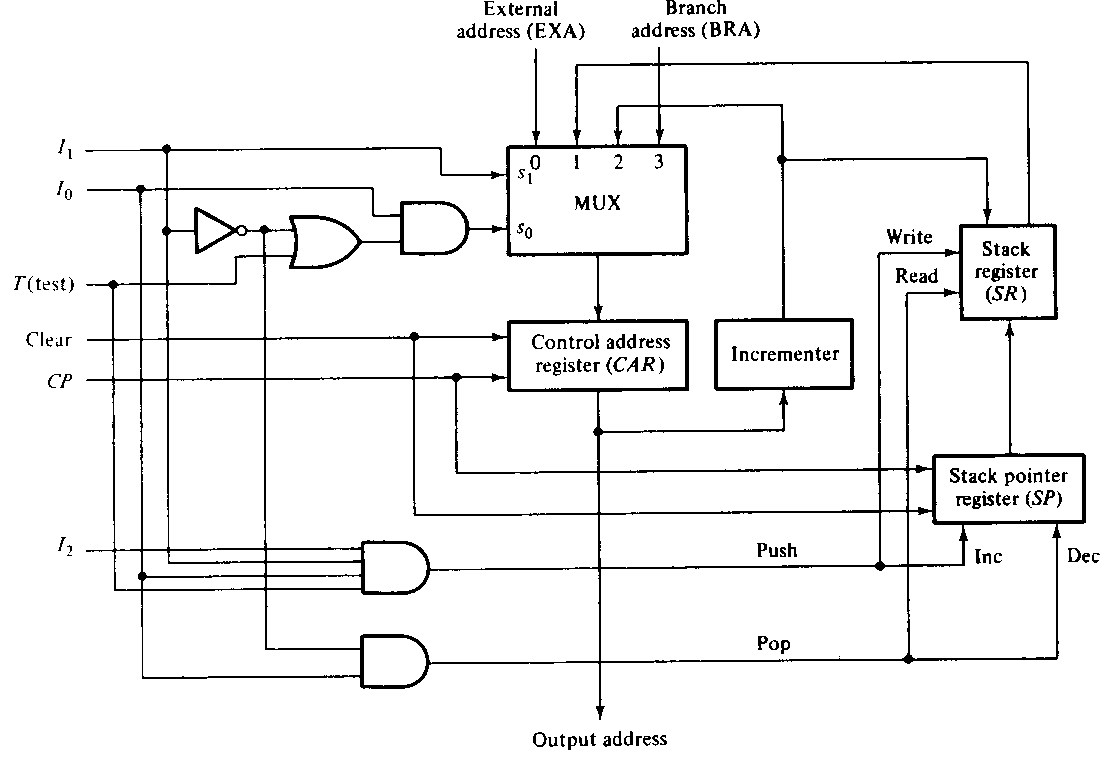






**19)** Explain the organization of a microprogrammed computer with a block diagram (10) **[Block diagram – 5 marks, Explanation – 5 marks]**

**20)** Draw a neat block diagram of a microprogram sequencer and explain its working. (10) **[Block diagram – 5 marks, Explanation – 5 marks]**



For the questions 18,19 & 20, Any relevant figure should be considered irrespective of text book….Hamacher or Morrismano.

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