Scheme of Valuation/Answer Key

(Scheme of evaluation (marks in brackets) and answers of problems/key)

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, MAY2019

Course Code: EC207

Course Name: LOGIC CIRCUIT DESIGN (EC, AE)

Max. Marks: 100		Duration: 3 Hours

PART A

		Answer any two full questions, each carries 15 marks.	Marks
1	a)	(a) 2 marks (b) 2 marks	(4)
	b)	specialty of Gray code-unit distance code (2 marks), practical application – for encoding angular position of a shaft with minimal error due to alignment mismatch (2 marks)	(4)
	c)	Relationship between error detection ability (D), error correction ability (C) and minimum distance (M) of a code C+D=M-1 (2 marks), Position of error C1C2C3 (3 marks), corrected code (2 mark)	(7)
2	a)	Proper K-map (3 marks), Output Y=CD+AB'+BD+A'B'C (4 marks)	(7)
	b)	Find the minimal sum of product of the following expression ABCD+AB'C'D'+AB'C+AB –Conversion to standard form (2 marks), K-map (2 marks), correct expression (4)	(8)
3	b)	Sign magnitude=10011001,1's complement=11100110, 2's complement=11100111	(5)
	b)	expressions for the output of a 1-bit magnitude comparator E=AB+A'B' (2 marks), L=AB' (3 marks), S=A'B (3 marks), Diagram (2 marks)	(10)

PART B

Answer any two full questions, each carries 15 marks.

4	a)	Differentiate between PLA and PAL with necessary diagrams	(7)
	b)	propagation delay (2 marks), power dissipation (2 marks), Fan-out (2 marks), comparison (2 marks)	(8)
5	a)	Explanation of race-around condition (2 marks), with waveform (1 mark), solution	(5)

		(2 marks)	
	b)	mod-6 synchronous counter using T-flip-flops-state diagram (2 marks), Excitation table (2 marks), K-maps (3 marks), excitation input expressions and diagram (3 marks)	(10)
6	a)	Diagram of TTL NAND gate with totem pole output (4 marks), the advantages and disadvantages (3 marks)	(7)
	b)	J K flip-flop using D flip-flops – Table (2 marks), K-map (2 marks), expression $D=Q_nK'+Q_n'J$ (2 marks), Diagram (2 marks)	(8)
PART C			
Answer any two full questions, each carries20 marks.			
7	a)	serial input parallel output (4 bit) shift register (5 marks), ring counter (5 marks)	(10)
	b)	block diagram of a finite state machine (2 marks), block diagram of Mealy machine (2) & Moore machine (2), comparison table (4)	(10)
8	a)	2 bit synchronous up/down counter-state diagram (2 marks), minimum state table (2 marks), three k-maps and expression for excitation inputs (3), diagram (3)	(10)
	b)	State reduction using implication chart	(10)
9	a)	the state diagram-3 states (2 marks), the minimum state table (2), excitation table (2), design using D flip-flop (2), Circuit (2)	(10)
	b)	different classes of shift registers (5 marks), use of parallel LOAD/SHIFT in shift registers (5 marks)	(10)
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