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| **Scheme of Valuation/Answer Key**  (Scheme of evaluation (marks in brackets) and answers of problems/key) | | | | | |
| **APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**  FIFTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018 | | | | | |
| **Course Code: EC361** | | | | | |
| **Course Name: DIGITAL SYSTEM DESIGN** | | | | | |
| Max. Marks: 100 | | |  | Duration: 3 Hours | |
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| **PART A** | | | | | |
|  |  | ***Answer any two full questions, each carries 15 marks.*** | | | Marks |
| 1 | a) | Next state and output equations----- 2.5 Marks  Excitation table---------- 2 Marks  Transition table---------- 2 Marks  State table-------------- 1.5 Marks  State diagram---------- 1 Mark | | | (9) |
|  | b) | ASM chart-------- 6 Marks | | | (6) |
| 2 | a) | Excitation/transition table------ 3.5 Marks  State table------- 2 Marks  Flow table------- 2.5 Marks  Flow diagram----- 1 Mark | | | (9) |
|  | b) | Multiple-row state assignment------ 2 Marks  Expanded flow table---------- 2 Marks  Transition table----------------- 2 Marks | | | (6) |
| 3 | a) | State diagram-------- 2 Marks  State table--------------- 1 Mark  Implication chart (reduction)------ 2.5 Marks  Minimal state table------------- 1.5 Marks | | | (7) |
|  | b) | ASM chart--------------- 3.5 Marks  Model type------------- 1.5 Marks | | | (5) |
|  | c) | Races---- critical & non-critical with example----- 1.5 Marks each | | | (3) |
| **PART B** | | | | | |
| ***Answer any two full questions, each carries 15 marks.*** | | | | | |
| 4 | a) | OR-AND implementation of the given function------- 1.5 Marks  Detection of Hazard using k-map--------------- 2.5 Marks  Hazard free implementation--------- 3 Marks | | | (7) |
|  | b) | Switch bouncing explanation with diagram---- 1.5 Marks  Solution (NAND latch)---- explanation with diagram and TT------ 2.5 Marks | | | (4) |
|  | c) | Essential Hazard---- explanation using suitable example (logic diagram)---- 4 Marks | | | (4) |
| 5 | a) | Set of all possible single stuck-at-faults and fault-free and faulty responses-------- 2 Marks  Fault cover table-------------- 2.5 Marks  Minimum test set------------------ 2.5 Marks | | | (7) |
|  | b) | a-test (SA0)--------- 4 Marks  b-test (SA1)------------- 4 Marks | | | (8) |
| 6 | a) | Jitter explanation with diagram------- 2 Marks, Sources----- 3 Marks( at least 4 sources) | | | (5) |
|  | b) | MOM explanation----- 2 Marks, diagram----- 2 Marks | | | (4) |
|  | c) | BIST techniques--- explanation with diagrams------ 6 Marks | | | (6) |
| **PART C** | | | | | |
| ***Answer any two full questions, each carries 20 marks.*** | | | | | |
| 7 | a) | Simple folding--------------- 2.5 Marks  Multiple folding--------------- 2.5 Marks  Bipartite folding--------------- 2.5 Marks  Constraint folding--------------- 2.5 Marks  OR  Row folding 5marks  Column folding –5 marks | | | (10) |
|  | b) | Architecture-------- 5 Marks  Explanation-------- 5 Marks | | | (10) |
| 8 | a) | Architecture-------- 5 Marks  Explanation-------- 5 Marks | | | (10) |
|  | b) | Concurrent testable PLA-------- 4 Marks  Parity testable PLA---------------- 4 Marks  Signature testable PLA------------ 2 Marks | | | (10) |
| 9 | a) | Fault models---- stuck-at faults, cross-point faults- extra and missing cross point fault( growth, shrinkage, appearance, disappearance faults)- explanation with an example------- 10 Marks | | | (10) |
|  | b) | Architecture-------- 5 Marks  Explanation-------- 5 Marks | | | (10) |
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