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| **APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**FOURTH SEMESTER B.TECH DEGREE EXAMINATION, APRIL 2018 |
| **Course Code: EC204** |
| **Course Name: Analog Integrated Circuit** |
| **Scheme of Valuation/Answer Key** |
| (Scheme of evaluation (marks in brackets) and answers of problems/key) |
| **PART A** |
| ***Answer any two full questions, each carries 15marks.*** |
| 1 | a) | Circuit diagram – (2), Working principle (1) , Analysis – (3), Transfer characteristics - (2) | (8) |
|  | b) | Circuit diagram – (2), Working principle & Analysis – (3), Condition – (2)  | (7) |
| 2 | a) | Circuit diagram – (1), Small signal Eq. Circuit (2) , Derivation of differential input resistance- (2), differential voltage gain – (2), Common mode gain – (2) | (9) |
|  | b) | Circuit - (2), explanation & advantage - (2), current gain – (2). | (6) |
| 3 | a) | Equivalent ckt - (3), derivation of closed loop voltage gain – (3), input resistance – (2) and output resistance – (2) | (10) |
|  | b) | maximum closed loop voltage gain = 40 | (5) |
| **PART B** |
| ***Answer any two full questions, each carries 15 marks.*** |
| 4 | a) | Circuit diagram – (3), Derivation – (5). | (8 ) |
|  | b) | Circuit diagram – (2), Design – (5). | (7) |
| 5 | a) | Circuit diagram - (2), working – (2), derivation - (4). | (8) |
|  | b) | Circuit - (3) working - (4) | (7) |
| 6 | a) | Circuit - (3) Derivation of the design equations – Transfer function, cut off frequency & closed loop gain (7) | (10) |
|  | b) | Circuit diagram – (2), Design – (3). | (5) |
| **PART C** |
| ***Answer any twofull questions, each carries 20 marks.*** |
| 7 | a) | Design a monostable multivibrator using 555 timer IC ( 741 op. amp. is also sufficient). Triggering signal is given 1KHz suare wave and quasiperiod is 0.3msec. Circuit diagram & justification – (4), Design – (3). | (7) |
|  | b) | Circuit with internal block diagram of the IC – (3), Explanation – (4). | (7) |
|  | c) | Block diagram / flow chart – (3), Principle – (3) | (6) |
| 8 | a) | Block diagram - (2), Working - (3) , capture range and lock range - (2) | (7) |
|  | b) | ExOR – (2), Principle with waveforms – (3) | (5) |
|  | c) | Circuit diagram - (3), Principle – (1), Design – (4). |  |
| 9 | a) | Dynamic range – 72.25dB – (2)Full-scale value – 9.9976V – (1)Resolution – 2.44mV – (2). | (5) |
|  | b) | Circuit – (3), Principle – (3) | (6) |
|  | c) | Block diagram – (3), Principle – (3), Derivation – (3) | (9) |
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