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| **unnamed**  **Scheme of Valuation/Answer Key**  (Scheme of evaluation (marks in brackets) and answers of problems/key) | | | | | |
| **APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**  IV SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018 | | | | | |
| **Course Code: EE204** | | | | | |
| **Course Name: Digital Electronics and Logic Design** | | | | | |
| Max. Marks: 100 | | |  | Duration: 3 Hours | |
| **PART A** | | | | | |
|  |  | ***Answer all questions, each carries5 marks.*** | | | Marks |
| 1 |  | Reason – 3 marks, Range – 2 mark | | | (5) |
| 2 |  | min terms-2.5 marks, MAX terms-2.5 marks | | | (5) |
| 3 |  | Derivation of sum and carry logic – 3 marks, circuit- 2 marks | | | (5) |
| 4 |  | Figure -2 marks, description of functioning- 3 marks | | | (5) |
| 5 |  | Figure- 2 marks, Truth table -2 marks, Explanation -1 mark | | | (5) |
| 6 |  | Definition -2 marks, Example with figure – 3 marks | | | (5) |
| 7 |  | Explanation -3 marks, Types-2marks | | | (5) |
| 8 |  | 5 differences – functional and implementation differences | | | (5) |
| **PART B** | | | | | |
| ***Answer any two full questions, each carries10 marks.*** | | | | | |
| 9 | a) | Binary to Gray – 2.5 marks Gray to Binary-2.5 marks | | | (5) |
|  | b) | K-map – 2 marks, Expression- 2 marks, Circuit – 1 mark | | | (5) |
| 10 | a) | Explanation (5) | | | (5) |
|  | b) | 5 different features – 5 marks each | | |  |
| 11 | a) | Explanation – 2marks, Examples- 2 marks | | | (4) |
|  | b) | K- map- 2marks, Expression -2 marks, NAND gate implementation – 2marks | | | (6) |
| **PART C** | | | | | |
| ***Answer any twofull questions, each carries10 marks.*** | | | | | |
| 12 | a) | Purpose – 2marks, Circuit – 4 marks, Explanation – 4 marks | | | (10) |
| 13 | a) | Simple Circuits of MUX & D-MUX- 2 marks each, Truth tables of MUX & D-MUX – 2 marks each, Explanation of differences- 1 mark | | | (5) |
|  | b) | Circuits of SR & JK FF-2 marks, Truth Tables – 2 marks, Diffrences – 1 mark | | | (5) |
| 14 | a) | Circuit- 4 marks, Truth table/ Timing diagram -4 marks, Explanation – 2marks | | | (10) |
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| **PART D** | | | | | |
| ***Answer any twofull questions, each carries 10 marks.*** | | | | | |
| 15 |  | Circuit- 4 marks, Truth table/ Timing diagram -4 marks, Explanation – 2marks | | | (10) |
| 16 | a) | Circuit- 2 marks, Truth table/ Timing diagram -2 marks, Explanation – 1marks | | | (5) |
|  | b) | Differences – 5 marks | | | (5) |
| 17 |  | i)Circuit- 2.5marks , Explanation – 2.5 marks  ii) Circuit- 2.5marks , Explanation – 2.5 marks | | | (10) |
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