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| **Scheme of Valuation/Answer Key****(Scheme of evaluation (marks in brackets) and answers of problems/key)** |
| **APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**THIRD SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018 |
| **Course Code: EC207** |
| **Course Name: LOGIC CIRCUIT DESIGN (EC, AE)** |
| Max. Marks: 100 |  | Duration: 3 Hours |
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| **PART A**  |
|  |  | ***Answer any two full questions, each carries 15 marks.*** | Marks |
| 1 | a) | i. 2 Marksii. 2 Marksiii. 2 Marksiv. 2 Marks | ( 8)  |
|  | b) | i. 2 Marksii. 2 Marksiii. 3 Marks | ( 7) |
| 2 | a) | i. Even parity 4 Marksii. Odd parity 4 Marks | (8) |
|  | b) | Block diagram 2 MarksOperation of MUX 2 MarksImplementation of the given function 3 Marks | (7) |
| 3 | a) | K map representation= 3 MarksSimplification= 3 Marks ( Term **“3”** should not be excluded) realization using NAND only= 4 Marks | (10) |
|  | b) | Logic diagram= 3 Marks, working= 2 Marks | (5) |
| **PART B**  |
| ***Answer any two full questions, each carries 15 marks.*** |
| 4 | a) | Circuit= 5Marks, Working = 5 Marks | ( 10) |
|  | b) | Comparison = 5 Marks | (5 ) |
| 5 | a) | Logic diagram= 5 Marks, Programming table = 3 Marks | (8) |
|  | b) | Truth table = 2 Marks, Design = 2 Marks, Logic circuit = 3 Marks | (7) |
| 6 | a) | Excitation table=3 Marks, Design using correct characteristic equation = 4 Marks Logic diagram= 3 Marks | (10) |
|  | b) | Conversion = 5 Marks | (5) |
| **PART C**  |
| ***Answer any two full questions, each carries20 marks.*** |
| 7 | a) | Complete PIPO register- Logic diagram= 7 Marks. Working= 3 Marks | (10) |
|  | b) |  Moore& Mealy sequential model with block diagrams =6 MarksComparison= 4 Marks | (10 ) |
| 8 | a) | Logic diagram of a Johnson counter.= 4 MarksTruth table= 3 MarksOperation = 3Marks | (10) |
|  | b) | i. 5 Marksii. 5 Marks | (10) |
| 9 | a) | 10 Marks, Proportional marks could be given for correct steps | (10) |
|  | b) | Sequence(flow) diagram =4 MarksFinal Logic diagram = 6 Marks | (10) |
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